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EXAMINER	
KIK, PHALLAKA	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,959	HENG ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2006 and 21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 31-36* is/are pending in the application, wherein claims 25-30 are cancelled.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to the RCE filed on 9/20/2006 and amendment after final filed on 8/21/2006. Claims 1-24,31-36 are pending, wherein claims 17,35 have been amended and claims 25-30 have been cancelled. Claims 1-24,31-36 have been examined. However, Applicant's arguments are not persuasive; therefore, the previous Office Action is incorporated herein.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/21/2006 has been entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. **Claims 1-24 and 31-36 are rejected under 35 U.S.C. 102(a)** as being anticipated by Regan (US Patent No. 6,756,242).

As per **claim 1**, Regan discloses a method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

defining technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

determining a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 1, line 27-31; col. 4, line 14-26; col. 4, line 52-60; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 1, line 27-31; col. 3, line 15-36; col. 4, line 52-60; col. 11, line 66-67; col. 13, line 5-13); and

in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

As per **claim 2**, Regan discloses the method of claim 1, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell (Fig. 20, #75; col. 1, line 7-16; col. 2, line 41-57; col. 7, line 7-12).

As per **claim 3**, Regan discloses the method of claim 1, wherein the placement and routing performing step includes using an optimization-based hierarchical scaling program to produce a legal layout for each problem object (col. 2, line 41-57; col. 8, line 6-11; Fig. 11; col. 8, line 41-44).

As per **claim 4**, Regan discloses the method of claim 1, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier (col. 2, line 26-40).

As per **claim 5**, Regan discloses the method of claim 1, wherein the identifying step includes:

manufacturing the design layout (col. 3, line 19-21);

testing the manufactured design layout and identifying at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

generating the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 6**, Regan discloses the method of claim 5, wherein the testing step includes characterizing operation and identifying the at least one problem object by obtaining data indicating how well objects are able to be manufactured (col. 10, line 41-53).

As per **claim 7**, Regan discloses the method of claim 5, wherein the manufacturing information generating step includes generating the scaling target for the problem object (Fig. 21, #81; col. 13, line 14-27).

As per **claim 8**, Regan discloses the method of claim 1, further comprising the step of evaluating whether a new design layout including the scaled objects achieves an expected behavior (Fig. 23; col. 14, line 34-67; Fig. 20, #75; col. 11, line 39-44).

As per **claim 9**, Regan discloses a system for selectively scaling an integrated circuit design layout (col. 10, line 27-36; col. 14, line 25-27), the system comprising the steps of:

means for identifying a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

means for defining technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

means for determining a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 4, line 14-26; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

means for determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 3, line 15-36; col. 11, line 66-67; col. 13, line 5-13); and

means for, in the case that assemble is required, performing placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

As per **claim 10**, Regan discloses the system of claim 9, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell (Fig. 20, #75; col. 1, line 7-16; col. 2, line 41-57; col. 7, line 7-12).

As per **claim 11**, Regan discloses the system of claim 9, wherein the placement and routing performing means includes means for conducting an optimization-based hierarchical scaling to produce a legal layout for each problem object (col. 2, line 41-57; col. 8, line 6-11; Fig. 11; col. 8, line 41-44).

As per **claim 12**, Regan discloses the system of claim 9, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier (col. 2, line 26-40).

As per **claim 13**, Regan discloses the system of claim 9, wherein the identifying means includes:

means for testing a manufactured design layout and identifying at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

means for generating the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 14**, Regan discloses the system of claim 13, wherein the testing means includes means for characterizing operation and identifying the at least one problem object by obtaining data indication how well objects are able to be manufactured (col. 10, line 41-53).

As per **claim 15**, Regan discloses the system of claim 13, wherein the manufacturing information generating means includes means for generating the scaling target for the problem object (Fig. 21, #81; col. 13, line 14-27).

As per **claim 16**, Regan discloses the system of claim 13, further comprising means for evaluating whether a new design layout including the scaled objects achieves an expected behavior. (Fig. 23; col. 14, line 34-67; Fig. 20, #75; col. 11, line 39-44).

As per **claim 17**, Regan discloses a computer program product comprising a computer useable medium having computer readable program code embodied therein for selectively scaling an integrated circuit design layout (col. 1, line 35-36; col. 2, line 5-6; col. 13, line 66 to col. 14, line 20), the program product comprising:

program code configured to identify a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

program code configured to define technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

program code configured to determine a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 4, line 14-26; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

program code configured to determine which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object

with a respective at least one scaling technique and scaling factor (col. 3, line 15-36; col. 11, line 66-67; col. 13, line 5-13) ; and

program code configured to, in the case that assembly is required, perform placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

As per **claim 18**, Regan discloses the program product of claim 17, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell (Fig. 20, #75; col. 1, line 7-16; col. 2, line 41-57; col. 7, line 7-12).

As per **claim 19**, Regan discloses the program product of claim 17, wherein the placement and routing performing code includes program code configured to conduct an optimization-based hierarchical scaling to produce a legal layout for each problem object (col. 2, line 41-57; col. 8, line 6-11; Fig. 11; col. 8, line 41-44).

As per **claim 20**, Regan discloses the program product of claim 17, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier (col. 2, line 26-40).

As per **claim 21**, Regan discloses the program product of claim 17, wherein the identifying code includes:

program code configured to test a manufactured design layout and identify at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

program code configured to generate the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 22**, Regan discloses the program product of claim 21, wherein the testing code includes program code configured to characterize operation and identify the at least one problem object by obtaining data indication how well objects are able to be manufactured (col. 10, line 41-53).

As per **claim 23**, Regan discloses the program product of claim 17, wherein the manufacturing information generating code includes program code configured to generate a scaling target for the problem object (Fig. 21, #81; col. 13, line 14-27).

As per **claim 24**, Regan discloses the program product of claim 17, further comprising program code configured to evaluate whether a new design layout including the scaled objects achieves an expected behavior (Fig. 23; col. 14, line 34-67; Fig. 20, #75; col. 11, line 39-44).

As per **claim 31**, Regan discloses a method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

defining technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

determining a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 1, line 27-31; col. 4, line 14-26; col. 4, line 52-60; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 1, line 27-31; col. 3, line 15-36; col. 4, line 52-60; col. 11, line 66-67; col. 13, line 5-13); and

in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

wherein the scaling factor includes at least one of a compensation and a new ground rule (col. 2, line 26-40).

As per **claim 32**, Regan discloses the method of claim 31, wherein the identifying step includes:

manufacturing the design layout (col. 3, line 19-21);

testing the manufactured design layout and identifying at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

generating the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 33**, Regan discloses a system for selectively scaling an integrated circuit design layout (col. 10, line 27-36; col. 14, line 25-27), the system comprising the steps of:

means for identifying a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

means for defining technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

means for determining a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 1, line 27-31; col. 4, line 14-26; col. 4, line 52-60; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

means for determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 1, line 27-31; col. 3, line 15-36; col. 4, line 52-60; col. 11, line 66-67; col. 13, line 5-13); and

means for, in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67).

wherein the scaling factor includes at least one of a compensation and a new ground rule (col. 2, line 26-40).

As per **claim 34**, Regan discloses the system of claim 33, wherein the identifying means includes:

means for testing a manufactured design layout and identifying at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

means for generating the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

As per **claim 35**, Regan discloses a computer program product comprising a computer useable medium having computer readable program code embodied therein for selectively scaling an integrated circuit design layout (col. 1, line 35-36; col. 2, line 5-6; col. 13, line 66 to col. 14, line 20), the program product comprising:

program code configured to identify a scaling target for at least one problem object of the design layout based on manufacturing information (Fig. 20, #70; col. 10, line 44-53; Fig. 21, #81; col. 13, line 5-15; col. 6, line 64 to col. 7, line 4);

program code configured to define technology ground rules and methodology constraints for each problem object (Abstract; col. 1, line 7-10; col. 1, line 27-31; col. 2, line 41-43; col. 2, line 58-60; Fig. 2; col. 5, line 63 to col. 6, line 9);

program code configured to determine a scaling factor for each problem object (Abstract; col. 1, line 10-16; col. 1, line 27-31; col. 4, line 14-26; col. 4, line 52-60; Fig. 20, #72; col. 10, line 66 to col. 11, line 3);

program code configured to determine which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor (col. 1, line 27-31; col. 3, line 15-36; col. 4, line 52-60; col. 11, line 66-67; col. 13, line 5-13); and

program code configured to, in the case that assembly is required, perform placement and routing to assemble the design using the scaled problem object (Abstract; col. 1, line 24-30; col. 4, line 40-67);

wherein the scaling factor includes at least one of a compensation and a new ground rule (col. 2, line 26-40).

As per **claim 36**, Regan discloses the program product of claim 35, wherein the identifying code includes:

program code configured to test a manufactured design layout and identify at least one problem object that is a problem (col. 10, line 34-40; col. 12, line 47-55); and

program code configured to generate the manufacturing information (Fig. 20, #73; col. 11, line 4-12).

Remarks

5. The objections of claims 17-21,35-36 due to the noted informalities are withdrawn as being corrected by Applicant's amendment filed on 8/21/2006.

6. Applicant argued that **Regan** fails to teach the determining of the a scaling factor for each problem object as claimed, wherein **Regan** only considers relationships among and between multiple parts (i.e., the whole chip), but not each individual problem object, and wherein **Regan** itself attempts to use the same scaling ratio for all the parts/components on an IC chip. The examiner is not persuaded in that Applicant's claimed invention is still unpatentable as being anticipated by the teachings of **Regan**, especially in the case when there is only "one problem object" in the IC design layout. First of all, although the Examiner agrees that **Regan** ultimately uses only a single scaling factor for scaling of the integrated circuit design layout, this single scaling factor is determined for the problem object(s) and applied to the problem object(s) using the selected scaling technique accordingly. Secondly, the term "problem object" does not confine to a single layout object since it could also refers to a type of problem in the whole or part of the IC layout. There is no limitation that only a particular part of the IC

layout to which scaling is applied; it is the "problem object" that defines the area to which scaling is being applied and not the area of the IC itself. Finally, "the at least one problem object" as recited in the claims, in the case that there is only one problem object or only one type of problem which would meet this claim limitation, there would necessarily be only one scaling factor (since a scaling factor is determined for each problem object as recited in the claim), which the method/system of **Regan** would anticipate as given in the previous rejection and incorporated herein as given above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action. In particular, the following prior arts are most relevant in teaching the determining of more than one scaling factors, including one different scaling factor for each problem object:

Kever et al. (U.S. Patent Application Publication No. 2005/0081167, especially paragraphs [0028], [0032], [0034], [0041]);

Allen et al. (U.S. Patent Application Publication No. 2004/0230922, especially paragraphs [0050]-[0053]);

Li (U.S. Patent Application Publication No. 2004/0064797, especially paragraphs [0041]-[0044], [0048], [0377]);

Meyer et al. (U.S. Patent Application Publication No. 2003/0217347, especially paragraphs [0041]);

Hall (US Patent No. 5,936,868, especially col. 3, line 3 to col. 5, line 10).

8. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

571-273-8300

Phallaka Kik
Primary Examiner
December 27, 2006